Amendments To The Claims

Please cancel Claims 1, 6, and 10-13 without prejudice. The following list of the claims replaces all prior versions and lists of the claims in this application.

1. (Canceled).

2. (Currently amended) The semiconductor device of ~~claim 1~~ claim 14 wherein there are at least two of the metallurgy layers that each include at least two of the dummy structures, and wherein at least two of the dummy structures on a first of the metallurgy layers are connected to at least two of the dummy structures on a second of the metallurgy layers through a plurality of vias.

3. (Currently amended) The semiconductor device of ~~claim 1~~ claim 14 wherein at least one of the one or more dummy structures comprises copper.

4. (Currently amended) The semiconductor device of ~~claim 1~~ claim 14 wherein at least one of the one or more dummy structures comprises aluminum.

5. (Currently amended) The semiconductor device of ~~claim 1~~ claim 14 wherein the distance between one of the dummy structures and one of the one or more conductive lines is at least 0.1μm.

6. (Canceled).

7. (Currently amended) The semiconductor device of ~~claim 1~~ claim 14 wherein there are at least two of the dummy structures that comprise different shapes.

8. (Currently amended) The semiconductor device of ~~claim 1~~ claim 14 wherein there are at least two of the dummy structures that comprise different materials.

9. (Currently amended) The semiconductor device of ~~claim 1~~ claim 14 wherein there are at least two of the dummy structures that comprise different sizes.

10. (Canceled).

11. (Canceled).

12. (Canceled).

13. (Canceled).

14. (Currently amended) ~~The semiconductor device of claim 12~~ An integrated circuit semiconductor device, comprising:

a semiconductor substrate;

one or more metallurgy layers connected to the semiconductor substrate, wherein each of the one or more metallurgy layers comprises one or more conductive lines and one or more dummy structures between the one or more conductive lines wherein at least two of the one or more dummy structures from different metallurgy layers are thermally connected; and

one or more dielectric layers between the one or more metallurgy layers;

wherein there are at least two of the dummy structures that are connected by a first line;

wherein the width of the first line is less than the width of each of the two dummy structures;

wherein the first line comprises aluminum;

wherein there are another two of the dummy structures that are connected by a second line; and

wherein the first line and the second line comprise different materials.

15. (Canceled).

16. (Canceled).

17. (Canceled).

18. (Canceled).

19. (Currently amended) ~~An integrated circuit~~ The semiconductor device~~, comprising: a semiconductor substrate; one or more metallurgy layers connected to the semiconductor substrate, wherein each of the one or more metallurgy layers comprises: one or more conductive lines; one or more dummy metal structures between the one or more conductive lines wherein at least two of the one or more dummy metal structures are connected by metal lines,~~ of Claim 14 wherein the distance between each of the dummy metal structures and each of the conductive lines is at least 0.1μm; and ~~one or more dielectric layers between the one or more metallurgy layers,~~ wherein the one or more dummy metal structures on a first metallurgy layer are connected to the one or more dummy metal structure on a second metallurgy layer through vias.

20. (Currently amended) The ~~integrated circuit~~ semiconductor device of claim 19 wherein the respective heights of the metal lines and the dummy metal structures are similar.